IN THE CLAIMS

1. (Previously Presented) A method of error detection in a computer processor having a plurality of memory elements, comprising:

computing a base digital root (DR) for each memory element having a value stored therein to form a corresponding base DR;

performing an operation on one or more of said memory elements to form a result;

performing said operation on one or more of said corresponding base DRs to form a check value;

computing a result DR of said result;

comparing said result DR to said check value; and

signaling an error based on said comparing, wherein

said computing a base DR and said computing a result DR each comprise: operating a set of input adders, each configured to add two 4-bit inputs and each configured to produce a single 4-bit output and a carry bit, and

operating a set of cascade adders operably connected to said 4-bit outputs and said carry bits of said set of input adders and configured to add said 4-bit outputs and said carry bits to produce the HDR of all of said 4-bit inputs without a carry bit,

wherein said set of input adders and said set of cascade adders operate combinatoricly.

2. (Original) The method of Claim 1, wherein said base DR is a hexadecimal digital root and said result DR is a hexadecimal digital root.

3. (Previously Presented) The method of Claim 1, wherein said performing an operation comprises any of the operations of adding, subtracting, integer multiplying, integer dividing, floating point multiplying and floating point dividing.

Claims 4-9. (Canceled)

10. (Original) The method of Claim 1, further comprising storing said corresponding base DR with each said memory element.

11. (Canceled)

12. (Previously Presented) A circuit apparatus for detecting errors in computer processor registers, comprising:

a first operation circuit operably connected to one or more of said registers and producing a first result;

one or more first hexadecimal digital root (HDR) circuits each operably connected to one of said registers, each producing a HDR for each said register;

a second operation circuit operably connected to said one or more first HDR circuits and producing a second result;

a second HDR circuit operably connected to said first operation circuit, receiving said first result and producing a result HDR;

a third HDR circuit operably connected to said second operation circuit, receiving said second result and producing a check HDR; and

a comparator operably connected to said second HDR circuit and said third HDR circuit, configured to compare said result HDR and said check HDR and producing an error flag, wherein said error flag indicates an error in said first operation circuit, wherein said first, second, and third HDR circuits each comprise:

a set of input adders, each configured to add two 4-bit inputs and each configured to produce a single 4-bit output and a carry bit, and

a set of cascade adders operably connected to said 4-bit outputs and said carry bits of said set of input adders and configured to add said 4-bit outputs and said carry bits to produce the HDR of all of said 4-bit inputs without a carry bit,

wherein said set of input adders and said set of cascade adders operate combinatoricly.

13. (Original) The circuit apparatus of Claim 12, wherein said first and second operation circuits perform the same operation, said operation selected from the group consisting of addition, subtraction, multiplication, division, and copying.

14. (Original) The circuit apparatus of Claim 12, wherein said HDR for each said register is stored with said register contents.

15. (Original) The circuit apparatus of Claim 12, wherein said first, second, and third HDR circuits are substantially identical.

16. (Canceled)

17. (Previously Presented) The circuit apparatus of Claim 12, wherein said set of input adders comprises eight adders.

18. (Previously Presented) The circuit apparatus of Claim 12, wherein said set of input adders comprises sixteen adders.

19. (Previously Presented) The circuit apparatus of Claim 12, wherein said set of cascade adders comprises:

a first tier of adders configured to sum said 4-bit outputs and said carry bits from said set of input adders into an intermediate set of sums and carry bits;

a second tier of adders configured to sum said intermediate set of sums and carry bits into a plurality of penultimate sums and carry bits;

a logic circuit configured to sum said plurality of penultimate sums and carry bits into a hexadecimal digital root.

20. (Original) The circuit apparatus of Claim 19, wherein said first tier of adders comprises eight 4-bit carry look-ahead adders.

21. (Original) The circuit apparatus of Claim 19, wherein said first tier of adders comprises sixteen 4-bit carry look-ahead adders.

22. (Previously Presented) An apparatus for error detection in a computer processor having a plurality of memory elements, comprising:

circuit means for computing a base digital root (DR) for each memory element having a value stored therein to form a corresponding base DR,

circuit means for performing an operation on one or more of said memory elements to form a result;

circuit means for performing said operation on one or more of said corresponding base DRs to form a check value;

circuit means for computing a result DR of said result;

circuit means for comparing said result DR to said check value; and

circuit means for signaling an error based on said comparing,

wherein said circuit means for computing a base DR and said circuit means for computing a result DR each comprise:

circuit means for operating a set of input adders, each configured to add two 4-bit inputs and each configured to produce a single 4-bit output and a carry bit, and

circuit means for operating a set of cascade adders operably connected to said 4-bit outputs and said carry bits of said set of input adders and configured to add said 4-bit outputs and said carry bits to produce the HDR of all of said 4-bit inputs without a carry bit,

wherein said set of input adders and said set of cascade adders operate combinatoricly.

23. (Original) The apparatus of Claim 22, wherein said base DR is a hexadecimal digital root and said result DR is a hexadecimal digital root.

24. (Previously Presented) The apparatus of Claim 22, wherein said circuit means for performing an operation comprises any of:

an adder;

a multiplier; and

a floating point multiplier.

Claims 25-26. (Canceled)

27. (Original) The apparatus of Claim 22, wherein said circuit means for performing an operation comprises means for moving the value in one of said memory elements into another said memory element.

Claims 28-29. (Canceled).

30. (Previously Presented) A computer system, comprising:

memory elements;

and a processor performing the steps of:

computing a base digital root (DR) for each memory element having a value stored therein to form a corresponding base DR;

performing an operation on one or more of said memory elements to form a result;

performing said operation on one or more of said corresponding base DRs to form a check value;

computing a result DR of said result;

comparing said result DR to said check value; and

signaling an error based on said comparing, wherein said computer instructions for computing a base DR and said computer instructions for computing a result DR each comprise:

computer instructions for operating a set of input adders, each configured to add two 4-bit inputs and each configured to produce a single 4-bit output and a carry bit, and

computer instructions for operating a set of cascade adders operably connected to said 4-bit outputs and said carry bits of said set of input adders and configured to add said 4-bit outputs and said carry bits to produce the HDR of all of said 4-bit inputs without a carry bit,

wherein said set of input adders and said set of cascade adders operate combinatoricly.

31. (Original) The computer system of Claim 30, wherein said base DR is a hexadecimal digital root and said result DR is a hexadecimal digital root.

32. (Previously Presented) The computer system of Claim 30, wherein said performing an operation comprises any of the operations of adding, subtracting, integer multiplying, integer dividing, floating point multiplying and floating point dividing.

Claims 33-38. (Canceled).

39. (Original) The computer system of Claim 30, further comprising computer instructions for storing said corresponding base DR with each said memory element.

40. (Canceled)

41 - 43. Cancelled

44-62. (Canceled)